**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claims 1 – 3.      (Canceled)

4.      (Currently Amended)      A pattern generating circuit ~~as set forth in claim 2,~~ comprising:

generating means for generating a logical pattern of correlated peak in a delay profile of a transmission path; and

removing means for sequentially removing a power component of the detected correlated peak from said delay profile using the logical pattern of said correlated peak generated by said generating means,

wherein said removing means selects a sample having the least delay period as a maximum point among samples by multiplying a preliminarily set given value to the maximum value among all samples.

5.      (Currently Amended)      A pattern generating circuit ~~as set forth in claim 2,~~ comprising:

generating means for generating a logical pattern of correlated peak in a delay profile of a transmission path; and

removing means for sequentially removing a power component of the detected correlated peak from said delay profile using the logical pattern of said correlated peak generated by said generating means,

wherein said removing means selects a sample having the most delay period as a maximum point among samples by multiplying a preliminarily set given value to the maximum value among all samples.

6.    (Currently Amended)    A pattern generating circuit ~~as set forth in claim 2,~~ comprising:

generating means for generating a logical pattern of correlated peak in a delay profile of a transmission path; and

removing means for sequentially removing a power component of the detected correlated peak from said delay profile using the logical pattern of said correlated peak generated by said generating means,

wherein said logical pattern is preliminarily generated on the basis of a coefficient set for a channel filter to be used for band restriction in said transmission path.

7.    (Currently Amended)    A pattern generating circuit as set forth in claim [[2]] 4,

wherein said logical pattern represent a peak shape in a single path of the delay profile.

8.    (Currently Amended)    A pattern generating circuit as set forth in claim [[2]] 4,

wherein said logical pattern represents the peak shape and side lobe contained therein in a single path of the delay profile.

Claims 9. – 11.    (Canceled).

12.    (Currently Amended)    A multi-path detection circuit ~~as set forth in claim 9,~~ for detecting a timing of multi-path by measuring a delay profile of a transmission path, comprising:

generating means for generating a logic pattern of a correlated peak in said delay profile; and

detection means for detecting position of the correlated peak on the basis of the logical pattern of the correlated peak generated by said generating means,

wherein said detection means selects a sample having the least delay period as a maximum point among samples by multiplying a preliminarily set given value to the maximum value among all samples.

13.     (Currently Amended)     A multi-path detection circuit ~~as set forth in claim 9,~~ for detecting a timing of multi-path by measuring a delay profile of a transmission path, comprising:

generating means for generating a logic pattern of a correlated peak in said delay profile; and

detection means for detecting position of the correlated peak on the basis of the logical pattern of the correlated peak generated by said generating means,

wherein said detection means selects a sample having the most delay period as a maximum point among samples by multiplying a preliminarily set given value to the maximum value among all samples.

14.     (Currently Amended)     A multi-path detection circuit ~~as set forth in claim 9,~~ for detecting a timing of multi-path by measuring a delay profile of a transmission path, comprising:

generating means for generating a logic pattern of a correlated peak in said delay profile; and

detection means for detecting position of the correlated peak on the basis of the logical pattern of the correlated peak generated by said generating means,

wherein said logical pattern is preliminarily generated on the basis of a coefficient set for a channel filter to be used for band restriction in said transmission path.

15.     (Currently Amended)     A multi-path detection circuit as set forth in claim [[9]] 12, wherein said logical pattern represent a peak shape in a single path of the delay profile.

16.    (Currently Amended)    A multi-path detection circuit as set forth in claim [[9]] 12, wherein said logical pattern represents the peak shape and side lobe contained therein in a single path of the delay profile.

17.    (Currently Amended)    A multi-path detection circuit as ~~set forth in claim 10, which~~ for detecting a timing of multi-path by measuring a delay profile of a transmission path, comprising:

generating means for generating a logic pattern of a correlated peak in said delay profile; and

detection means for detecting position of the correlated peak on the basis of the logical pattern of the correlated peak generated by said generating means,

wherein said detection means comprises removing means for sequentially removing power component of the detected correlated peak from said delay profile using the logical pattern of said correlated peak and means for sequentially detecting the position of said correlated peak from the delay profile by removing the power component of the correlated peak by said removing means,

wherein said multi-path detection circuit further comprises:

position interval judgment means for detecting interval of positions of said correlated peaks, and wherein removal of power component of said correlated peak is performed by said removing means depending upon the result of judgment of said position interval judgment means.

Claims 18. – 20.    (Canceled)

21.    (Currently Amended)    A multi-path detection circuit ~~as set forth in claim 18,~~ comprising:

a matched filter outputting a correlated value of a spread code and a received signal;

delay profile storing means for storing a delay profile of a transmission path measured by said matched filter;

maximum value retrieving means for retrieving a maximum peak position and a peak level from said delay profile stored in said delay profile storing means;

pattern generating means for sequentially generating logical patterns of correlated peaks on the basis of the peak level and peak position obtained from said maximum value retrieving means; and

preparing means for preparing a profile by removing a correlation power of the peak retrieved at preceding time by said maximum value retrieving means;

said maximum value retrieving means retrieves said maximum peak value and said peak level sequentially from the profile generated by said pattern generating means,

wherein said maximum value retrieving means comprises:

level comparing means for comparing a delay profile data samples and an interim maximum value amount retrieved samples;

selecting means for selecting one of said delay profile data sample and said interim maximum value depending upon the result of comparison by said level comparing means;

buffer means for storing said interim maximum value during maximum value retrieval; and

maximum position holding means for outputting a maximum peak position by holding a sample position upon detecting of new maximum value by said level comparing means.

22.    (Original)    A multi-path detection circuit as set forth in claim 21, wherein said maximum value retrieving means includes coefficient calculating means for performing calculation of a preliminarily set given value and a interim maximum value stored in said buffer means, and selecting a sample having the least delay period as a maximum point among samples on the basis of a result of calculation by said coefficient calculation means.

23.    (Currently Amended)    A multi-path detection circuit as set forth in claim 21, wherein said maximum value retrieving means includes coefficient calculating means for performing calculation of a preliminarily set given value and [[a]] an interim maximum value stored in said buffer means, and selecting a sample having the most delay period as a maximum point among samples on the basis of a result of calculation by said coefficient calculation means.

24.    (Currently Amended)    A multi-path detection circuit as set forth in claim 18, comprising:

a matched filter outputting a correlated value of a spread code and a received signal;

delay profile storing means for storing a delay profile of a transmission path measured by said matched filter;

maximum value retrieving means for retrieving a maximum peak position and a peak level from said delay profile stored in said delay profile storing means;

pattern generating means for sequentially generating logical patterns of correlated peaks on the basis of the peak level and peak position obtained from said maximum value retrieving means; and

preparing means for preparing a profile by removing a correlation power of the peak retrieved at preceding time by said maximum value retrieving means;

said maximum value retrieving means retrieves said maximum peak value and said peak level sequentially from the profile generated by said pattern generating means,

wherein said pattern generating means comprises a logical pattern memory storing a preliminarily set logical pattern, setting means for setting a peak level using a logical pattern stored in said logical pattern memory, and peak position setting means for setting a position of the correlated peak from a peak position input and peak shape output from said setting means.

25.    (Currently Amended)      A multi-path detection circuit as set forth in claim [[18]] 21, wherein said preparing means ~~preparing~~ prepares a profile from which has been removed the correlated power of the peak retrieved preceding time by said maximum value retrieving means by removing the logical pattern of the correlated peak generated by said pattern generating means from the delay profile data retrieved with said maximum peak position and said peak level by said maximum value retrieving means.

26.    (Currently Amended)      A multi-path detection circuit ~~as set forth in claim 18,~~ comprising:

a matched filter outputting a correlated value of a spread code and a received signal;

delay profile storing means for storing a delay profile of a transmission path measured by said matched filter;

maximum value retrieving means for retrieving a maximum peak position and a peak level from said delay profile stored in said delay profile storing means;

pattern generating means for sequentially generating logical patterns of correlated peaks on the basis of the peak level and peak position obtained from said maximum value retrieving means; and

preparing means for preparing a profile by removing a correlation power of the peak retrieved at preceding time by said maximum value retrieving means,

wherein said logical pattern is preliminarily generated on the basis of a coefficient set in a channel filter used for band restriction in said transmission path.

27.    (Currently Amended)      A multi-path detection circuit as set forth in claim [[18]] 26, wherein said logical pattern represents a peak shape in a single path of said delay profile.

28. (Currently Amended) A multi-path detection circuit as set forth in claim [[18]] 26, wherein said logical pattern represents a peak shape and a side lobe contained therein in a single path of said delay profile.

29. (Original) A multi-lobe detection circuit as set forth in claim 18 which further comprises comprising:

a matched filter outputting a correlated value of a spread code and a received signal;

delay profile storing means for storing a delay profile of a transmission path measured by said matched filter;

maximum value retrieving means for retrieving a maximum peak position and a peak level from said delay profile stored in said delay profile storing means;

pattern generating means for sequentially generating logical patterns of correlated peaks on the basis of the peak level and peak position obtained from said maximum value retrieving means;

preparing means for preparing a profile by removing a correlation power of the peak retrieved at preceding time by said maximum value retrieving means; and

position interval judgment means for detecting interval of positions of said correlated peaks, and priparing wherein preparing of a profile from which is removed said correlated power of the peak retrieved preceding time is performed by said priparing preparing means depending upon the result of judgment of said position interval judgment means.

Claims 30. – 32. (Canceled)

33. (Currently Amended) A multi-path detection method as set forth in claim 30, for detecting a timing of multi-path by measuring a delay profile of a transmission path, comprising the steps of:

generating a logical pattern of a correlated peak in a delay profile; and

detecting a position of correlated peak on the basis of the generated logical pattern of said correlated peak,

wherein said step of detecting position of said correlated peak selects a sample having the least delay period as a maximum point among samples by multiplying a preliminarily set given value to the maximum value among all samples.

34. (Currently Amended) A multi-path detection method as set forth in claim 30, for detecting a timing of multi-path by measuring a delay profile of a transmission path, comprising the steps of:

generating a logical pattern of a correlated peak in a delay profile; and

detecting a position of correlated peak on the basis of the generated logical pattern of said correlated peak,

wherein said step of detecting position of said correlated peak selects a sample having the most delay period as a maximum point among samples by multiplying a preliminarily set given value to the maximum value among all samples.

35. (Currently Amended) A multi-path detection method as set forth in claim 30, for detecting a timing of multi-path by measuring a delay profile of a transmission path, comprising the steps of:

generating a logical pattern of a correlated peak in a delay profile; and

detecting a position of correlated peak on the basis of the generated logical pattern of said correlated peak,

wherein said logical pattern is preliminarily generated on the basis of a coefficient set for a channel filter to be used for band restriction in said transmission path.

36.    (Currently Amended)    A multi-path detection method as set forth in claim [[30]] 33, wherein said logical pattern represent a peak shape in a single path of the delay profile.

37.    (Currently Amended    A multi-path detection method as set forth in claim [[30]] 33, wherein said logical pattern represents the peak shape and side lobe contained therein in a single path of the delay profile.

38.    (Currently Amended)    A multi-path detection method as set forth in claim 31, for detecting a timing of multi-path by measuring a delay profile of a transmission path, comprising the steps of:
       generating a logical pattern of a correlated peak in a delay profile; and
       detecting a position of correlated peak on the basis of the generated logical pattern of said correlated peak,
       wherein said step of detecting position of said correlated peak position includes step of sequentially removing power component of the detected correlated peak from said delay profile using the logical pattern of said correlated peak and step of sequentially detecting the position of said correlated peak from the delay profile removed the power component of the correlated peak, and
       wherein position internal of said correlated peaks are detected to remove power component of the detected correlated peak from the delay profile sequentially depending upon the result of judgment.